IN THE SPECIFICATION:

Please amend the paragraph starting at page 51, line 24 and ending at page 52, line 5, as follows:

--At time t2, similarly, the line V2 is selected, and when the control signals ϕTG1'', ϕTG2', ϕTB1 and ϕTB2 are set to level H, the pixel signal G22 is transferred to the upper memories MG21 and MG22, and the pixel signal B21 is transferred to the lower memories MB11 ~~MR11~~ and MB12 ~~MR12~~. The upper ~~lower~~ two memories MB21 and MG22 and the lower ~~upper~~ memories MB11 and MB12 are employed in common to increase the gain for reading from the memory to the horizontal output line.--

Please amend the paragraph starting at page 75, line 7 and ending at line 16, as follows:

--With this arrangement, transfer gates 423a to 423d, an FD 425, an input gate 426 of a source follower, and a reset MOS gate 433 are all located under horizontal lines (scanning lines 428a to 428d, a row selection line 430 and a reset line 432). Therefore, the size of the photodiodes 422a to 422d and the aperture ratio can be maximized. Further, the openings are continuously arranged in the center of the individual pixels, and a light shielding portion is formed in the horizontal and vertical line areas 427, 431 and 421 ~~area~~.--